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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,743	03/06/2002	Danielle A. Thomas	01-C-086 (STMI01-01086)	8460

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EXAMINER	
NGUYEN, DONGHAI D	
ART UNIT	**PAPER NUMBER**
3729	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,743	THOMAS ET AL.	
	Examiner	Art Unit	
	Donghai D. Nguyen	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The proposed reply filed on July 06, 2004 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "a portion ... circuit area" (claim 1, lines 3-4) is vague and indefinite, since it is unclear as to what made of the portion the integrated circuit. Does it comprise only the active circuit area or other element to form the portion? Furthermore, it is unclear as to what made of redistribution metal layer. Does it includes only the area where the solder connection is disposed or it comprises the metal layer in the via/hole and/or plug and/or metal pad?

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims1-3, 5-8, 10-13, 15-17, 19-20, and 22 as best understood are rejected under 35 U.S.C. 102(e) as being anticipated by Toyosawa et al.

Regarding claims 1 and 10, Toyosawa et al disclose an integrated circuit and a method for fabricating an integrated circuit comprising the steps of: fabricating a portion (active element 20, barrier layer 13) of the integrated circuit (Fig. 1), the portion comprising at least one active circuit area (20); and fabricating a redistribution metal layer (second metal layer 14, barrier layer 13) at least partially (barrier layer 13, first metal layer 9a, 9b) during fabrication of the portion of the integrated circuit;

Regarding claims 2, 6, 12, 20, and 22, Fig. 1 shows portion of the redistribution metal layer that are open to receive a solder bump (30).

Regarding claims 3 and 13, Toyosawa et al disclose the steps of: fabricating the active circuit area (20) and an associated metal pad (9a, b) on a base substrate (1); fabricating a vertical plug (vertical portion of part 14); mounting the vertical plug in electrical connection with the metal pad (Fig. 4f); depositing an undoped silicon oxide layer (10a) on the active circuit area and on a portion of the metal pad; depositing a phosphosilicate glass layer (10b) on the undoped silicon oxide layer; depositing a silicon oxynitride layer (10c) over the phosphosilicate glass layer; depositing a flat metal layer (14) over the silicon oxynitride layer; and in electrical connection with the vertical plug (Fig. 4f).

Regarding claims 5, 7-8, and 15-17, Toyosawa et al disclose the steps of: fabricating the active circuit area (20) and an associated metal pad (9a,b) on a base substrate (1); depositing an undoped silicon oxide layer (10a) on at least a portion active circuit area and on said metal pad;

depositing a phosphosilicate glass layer (10b) on the undoped silicon oxide layer; depositing a metal layer (14) over the phosphosilicate glass layer and electrical connection with the metal pad; and depositing a silicon oxynitride layer (15) over at least some portions of the metal layer (Fig. 13 b).

Regarding claim 10 and 19, Figs. 4f and 13b show the redistribution metal layer using a last metal layer that is used to fabricate the active circuit area of the integrated circuit.

Allowable Subject Matter

6. Claims 4, 9, 14, 18, and 21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed July 06, 2004 have been fully considered but they are not persuasive.

Applicants argue that Toyosawa clearly fails to anticipate fabricating a redistribution metal layer at least partially during fabrication of a portion of an integrated circuit. The Examiner respectfully disagrees. Toyosawa discloses the portion of the integrated circuit, which includes the first metal layer (9a, 9b) and barrier (13), and also discloses the redistribution metal layer, which also comprises the first metal layer (9a, 9b) and barrier (13), therefore the fabrication of redistribution layer is partially overlaps with the fabrication of the portion of the integrated circuit. Furthermore, Applicants' Figs. 4 and 8 show the step of fabricating active

circuit area (step 410 and 810) is separated (not partially overlap) from step of fabricating the redistribution metal layer (step 430 and 850). Moreover, the argument is considered to be met and inclusive in view of the rejections set forth above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (703) 305-7859. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (703) 308-1789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN

A. DEXTER TUGBANG
PRIMARY EXAMINER